CLAIM LISTING:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A content addressable memory, comprising:

at least one tag input;

at least one output;

at least one random access memory; and

circuitry to:

perform multiple read operations of the at least one random access memory, different ones of the read operations specifying an address based on different subsets of ~~tag~~ bits of a tag; and

based on the multiple read operations, generate at least one signal via the at least one output.

2. (Original) The content addressable memory of claim 1, wherein the at least one signal comprises at least one signal selected from the following group: a hit signal and an entry number signal.

3. (Original) The content addressable memory of claim 1, wherein the at least one random access memory comprises multiple random access memories.

4. (Currently Amended) The content addressable memory of claim 3,

wherein ~~the~~ a number of tag subsets used in the multiple read operations is equal to the number of random access memories.

5. (Currently Amended) The content addressable memory of claim 4,

wherein each of the subsets of ~~tag~~ bits of the tag forms an address applied to each of the respective random access memories.

6. (Original) The content addressable memory of claim 1,

wherein the multiple read operations comprise more than one read operation applied to the same random access memory.

7. (Original) The content addressable memory of claim 6,

wherein individual ones of the more than one read operations applied to the same random access memory specify an address based on a subset of the tag value and an identifier of a section of the random access memory

8. (Original) The content addressable memory of claim 1, wherein the circuitry is constructed to perform at least two of the read operations in parallel.

9. (Original) The content addressable memory of claim 1,

wherein the circuitry further comprises circuitry to set bits of the at least one random access memory in response to a tag value to be written to the content addressable memory.

10. (Original) The content addressable memory of claim 9,

wherein the tag value to be written comprises a ternary tag value including at least one "don't care" bit; and

wherein the circuitry to set bits comprises circuitry to set bits for different values of the "don't care" bit.

11. (Currently Amended) The content addressable memory of claim 1,

wherein the at least one random access memory stores data at each address identifying entries sharing a value of a subset of the ~~tag~~ bits of the tag.

12. (Currently Amended) A content addressable memory, comprising:

at least one tag input;

multiple random access memories, each memory corresponding to a different set of bit positions within a tag;

circuitry to:

apply different subsets of the ~~tag~~ bits of the tag as addresses to the different respective random access memories in read operations; and

AND output of the random access memories in response to the read operations.

13. (Original) The content addressable memory of claim 12, further comprising an encoder to encode the results of the AND.

14. (Original) The content addressable memory of claim 13, wherein the circuitry to encode the results comprises at least one selected from the following group: a network of at least one OR gate to operate on the results of the AND-ing, and a one-hot to binary encoder.

15. (Original) The content addressable memory of claim 12, wherein the circuitry further comprises circuitry to set at least one bit in each of the multiple random access memories based on a tag value to write.

16. (Original) The content addressable memory of claim 15, wherein the circuitry to set at least one bit comprises circuitry to write multiple bits based on a ternary tag value.

17. (Currently Amended) A method, comprising:

dividing a received content addressable memory lookup tag value into multiple subtags values;

performing multiple read operations of at least one random access memory using addresses based on the multiple, respective, subtag values; and

based on the read operations, determining which, if any, entries feature each of the multiple subtags; and

outputting at least one indication in response to the determining.

18. (Original) The method of claim 17, wherein performing multiple read operations comprises using each of the multiple subtags as at least a portion of an address specified in the read operations.

19. (Original) The method of claim 17, wherein the at least one random access memory comprises multiple random access memories.

20. (Original) The method of claim 19, wherein the multiple random access memories store a bit vector of entry values at subtag addresses.

21. (Original) The method of claim 17, further comprising:

receiving a tag to write; and

setting bits in the at least one random access memory based on the received tag.

22. (Original) The method of claim 21,

wherein receiving a tag comprises receiving a tag including at least one "don't care" bit; and

wherein the setting bits comprises writing entry data associated with multiple values of the same subtag within a one of the at least one random access memories.

23. (Currently Amended) A network forwarding device, comprising:

a switch fabric; and

multiple line cards interconnected by the switch fabric, individual ones of the line cards comprising:

at least one network port; and

circuitry to process packets received via the at least one port, the digital logic circuitry including a content addressable memory, the content addressable memory comprising:

at least one tag input;

at least one output;

at least one random access memory;

content addressable memory circuitry to:

perform multiple read operations of the at least one random access memory, different ones of the read operations specifying an address based on different subsets of the ~~tag~~ bits of a tag; and

based on the multiple read operations, generate at least one signal via the at least one output.

24. (Original) The network forwarding device of claim 23, wherein at least one of the line cards comprises a network processor having multiple multi-threaded engines integrated on a single die.